REMARKS

35 USC 103

Applicant respectfully continues to traverse the Examiner's rejections, and reincorporates Applicant's comments in the response filed on 10/05/06.

In addition, Applicant appreciates the Examiner's consideration of the following comments. ZHU patent # 5866924 is a method and apparatus for routing or wiring a clock net in an integrated circuit device. The Patent teaches how to determine balance points for branches of a net and line segments to connect the points such that the sinks will all have the same timings or meet timing requirements from a source.

Carrig et al patent # 5339253 teaches how to change connections of equivalent sources and sinks to achieve better skew with reduce delay and power. Generating circuits can be added as necessary to improve the solution.

Bergeron et al 6609228 B1here Bergeron's Patent is an extension of the Carrig et al patent. The patent teaches how to change connections of equivalent sources and sinks similar to Carrig however it does additional arrangements to reduce power. For example it teaches that sinks can be placed in a row or column with the driving circuit in the center of those sinks. This can save considerable power since the latches account for much power of a clock tree.

Arthanari et al patent solves a very different problem than ZHO or Carrig or Bergeron or any combination of each patent. Arthanari patent is for a clock floor planner. The patent teaches how to use non homogenous clock books of different sizes and aspect ratios to their advantage for power or performance and how to select and place into the spaces on a complex integrated circuit with many floor planned elements such as the IP blocks of an ASIC or microprocessor. This finds a high speed or low power clock solution independently of all of the other datapath floorplaning that is required to close timing and power constraints. The patent teaches how to add symmetry.

Thus, applicant reasserts that: (1) the drive points described in the '253 patent are connect points for the wires and are not placement points for clock sources as set forth in Applicant's claim 1 (e.g., "connecting a source of clock signals"), and (2) the drive points described in the '924 patent are connect points for the wires, and not placement points for clock sources as set forth in Applicant's claim 1.

Allowance is solicited.

Respectfully submitted,
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